T-43-24

GigaBit Logic

16G010
16G011

Programmable
GaAs Schottky Diode Arrays

FEATURES

- 14 Schottky barrier diodes and one full wave rectifier on each chip
- 15 mA (16G010) and 100 mA (16G011) versions
- Very low junction capacitance
- Low series resistance
- Excellent thermal and electrical matching
- 150 GHz typical RC cutoff frequency
- Available with personalized interconnects in the package for design integration and improved performance
- Available in leadless chip carrier (LCC), flatpack, or die form.

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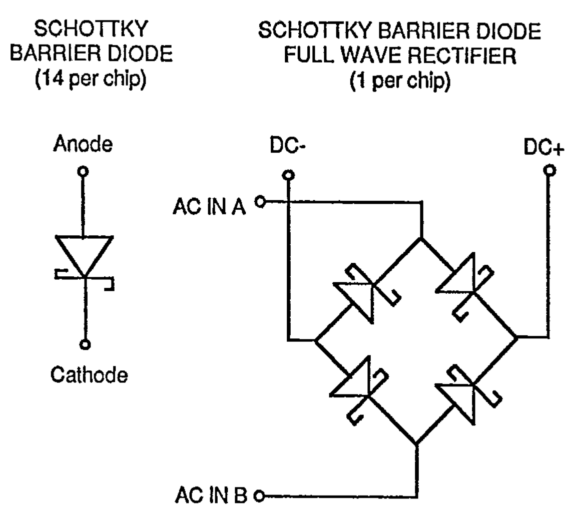
APPLICATIONS

- Sample and Hold Amplifiers
- High speed switching
- Waveform clamps
- High frequency mixers
- Video to microwave detectors
- Harmonics generators
- Input overload protection devices for electrostatic discharge (ESD) or RF overload
- Low capacitance varactors

FUNCTIONAL DESCRIPTION

The 16G010 and 16G011 are respectively, 15 mA and 100 mA GaAs Schottky barrier diode arrays. Each array consists of 14 individual diodes plus a full wave rectifier. Both arrays feature exceedingly low junction capacitance (0.042 pf typ. for the 16G010 and 0.12 pf typ. for the 16G011) and low series resistance (25Ω typical @ If = 5mA for the 16G010 and 7Ω typical @ If =30mA for the 16G011). The 3 dB cut-off frequency is 150 GHz for the 16G010 and 190 GHz for the 16G011. It is lower for packaged parts due to package capacitance. In order to take better advantage of the high frequency characteristics of the diodes in the 16G010/16G011, GigaBit offers the option to interconnect Diodes and add chip components as necessary inside the package (LCC or Flatpack). Package parasitic capacitance and inductance generally limits the performance of packaged parts. By interconnecting the Diodes inside the package to form a personalized analog function, the overall effect of package parasitic impedance is reduced since there is less I/O per function. The 16G010 and 16G011 are fabricated using GigaBit Logic GaAs planar process technology.

16G010, 16G011 CIRCUIT DIAGRAM



ORDERING INFORMATION

PACKAGE TYPE	16G010	16G011
36 pin Leadless CC	16G010-L36	16G011-L36
36 pin Flatpack	16G010-F	16G011-F
Die	16G010-X	16G011-X

ORDERING INFORMATION

16G010/16G011 DIODE ARRAY PERSONALIZATIONS

Please contact factory for special part number.

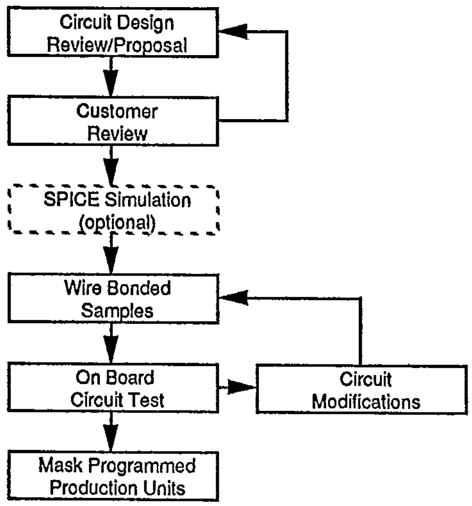
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CIRCUIT DESIGN INTEGRATION USING PERSONALIZED 16G010/16G011

GigaBit Logic can integrate certain analog designs by utilizing the 14 Diodes in the 16G010/16G011. Chip resistors and capacitors can also be added in the package cavity to realize more complex circuits. By interconnecting 16G010/16G011 Diodes inside the package, GigaBit can offer personalized analog functions with better performance than when the interconnects are external. First, the effect of package and wire bonds parasitic capacitance and inductance is reduced since there are fewer I/O per function. Chip capacitors and resistors can be attached close to the die bond pads in order to minimize wire bond length. Second, since there are fewer overall I/O per package, it is possible to adopt a Ground-Signal-Ground approach for the pin-out. This lowers cross capacitance between adjacent pins reducing cross talk as well as potential jitter in the circuit.

DESIGN INTEGRATION PROGRAM FLOW



PROGRAM FLOW FOR PROTOTYPES

GigaBit will review or propose a circuit schematic to personalize the 16G010/16G011 to the desired function. Prototypes are custom wire-bonded during assembly. Chip resistors and capacitors are added in the package as necessary. This approach has two main advantages: no Non-Recurring Engineering Expenses (NRE) and a quick turnaround time (2 to 4 weeks). Since there is no NRE, designers have total flexibility to try out a design and modify it if necessary.

GigaBit can provide, as an option, complete simulation of the circuit utilizing its proprietary spice model.

PROGRAM FLOW FOR PRODUCTION DEVICES

Production devices are customized via mask programming. The interconnects are realized in the IC substrate by changing the top metal layer mask of the 16G010/16G011.

Mask programming for production devices is advised to improve reliability and reproducibility compared with wire bonded prototypes. In addition, mask programmed ICs require less assembly work and are lower in cost compared with wire bonded prototypes.

EXAMPLES

Applications that can be integrated using the 16G010/16G011 Diode arrays include:

- Sample and hold amplifiers
- High frequency detectors
- Input overload protection diodes

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16G011

ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired)		
SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
I_F	Forward Current 16G010	28 mA
	16G011	200 mA
V_R	Reverse Bias Voltage	18 V
V_{ISOL}	Isolation Voltage Between Diodes	50 V
P_D	Maximum Power Dissipation -- per chip 16G010	1.5 W
	10G011	1.5 W
	-- per diode 16G010	100 mW
	16G011	500 mW
T_{STOR}	Storage Temperature	- 65 °C to + 150 °C

16G010L, 16G010F, 16G010X ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_F	Forward Voltage (Note 2)	I_F = 1 mA	0.68	0.73	0.78	V
		I_F = 5 mA		0.82	0.92	V
		I_F = 15 mA		0.96	1.1	V
V_{FM}	Forward Voltage Match	I_F = 5 mA		9	20	mV
I_R	Reverse Current	V_R = 4 V		0.01	1.0	µA
V_{BR}	Breakdown Voltage	I_R = 15 µA	6.0	8.0		V
V_{ISOL}	Isolation Voltage Between Diodes	I = 15 µA		40		V
I_{ISOL}	Leakage current Between Diodes	V = 30 V			1.0	µA
I_F+I_R	Forward + Reverse Current	V_F = 230 mV		60		nA
$C_{jo} + C_p$	Junction plus Parasitic Capacitances (Note 3)	DIE, V_F = 0 V		0.042		pF
R_S	Series Resistance	I_F = 1mA, 3mA, 5mA		25	35	Ω
$\Delta V / \Delta T$	Temp. Coeff of Forward Voltage Match	T_A = 0 °C to 85 °C		±20		µV/°C
$\frac{1}{2\pi R_S C_{jo}}$	Series RC Cutoff Frequency (Note 3)	DIE		150		GHz

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16G011L, 16G011F, 16G011X
ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_F	Forward Voltage (Note 2)	$I_F = 5$ mA	0.60	0.68	0.76	V
		$I_F = 15$ mA		0.76	0.88	V
		$I_F = 30$ mA		0.82	0.94	V
		$I_F = 50$ mA		0.89	1.01	V
		$I_F = 100$ mA		1.06	1.18	V
V_{FM}	Forward Voltage Match	$I_F = 50$ mA		8	20	mV
I_R	Reverse Current	$V_R = 4$ V		0.01	5.0	µA
V_{BR}	Breakdown Voltage	$I_R = 100$ µA	6.0	7.0		V
V_{ISOL}	Isolation Voltage Between Diodes	I = 100 µA		40		V
I_{ISOL}	Leakage current Between Diodes	V = 30 V			1.0	µA
$I_F + I_R$	Forward + Reverse Current	$V_F = 230$ mV		60		nA
$C_{jo} + C_p$	Junction plus Parasitic Capacitances (Note 3)	DIE, $V_F = 0$ V		0.12		pF
R_S	Series Resistance	$I_F = 15$mA, 30mA, 50mA		7	25	Ω
$\Delta V / \Delta T$	Temp. Coeff of Forward Voltage Match	$T_A = 0$ °C to 85 °C $I_F = 50$ mA		±20		µV/°C
$\frac{1}{2\pi R_S C_{jo}}$	Series RC Cutoff Frequency (Note 3)	DIE		190		GHz

NOTES:

1. Test conditions, unless otherwise stated: TA = 25°C
2. Max V_F for single diodes only. For Diode Bridge add 0.05 V.
3. For packaged parts, the measured capacitances will be increased by both shunt capacitance (C1G from each pin to ground) and interelectrode capacitance (C12, between adjacent pins). For the flatpack (assuming 0.150" external leads), the shunt capacitance is C1G = 0.25 pf and the interelectrode contribution is C12 = 0.20 pf. In addition, each lead has a series inductance of about 7nH in the flatpack (including the 0.150" Leads). For the leadless chip carrier package these values are C1G = 0.5 pf shunt and C12 = 0.1 pf, with a series inductance of 4nH on each lead. The shunt capacitances are principally to the ground pin on the package, which should be connected to an AC ground to minimize high frequency crosstalk between diodes.
4. Cj can be calculated as follows:

$$C_j = \frac{C_{jo}}{\sqrt{1 - \frac{V_D}{0.85}}}$$

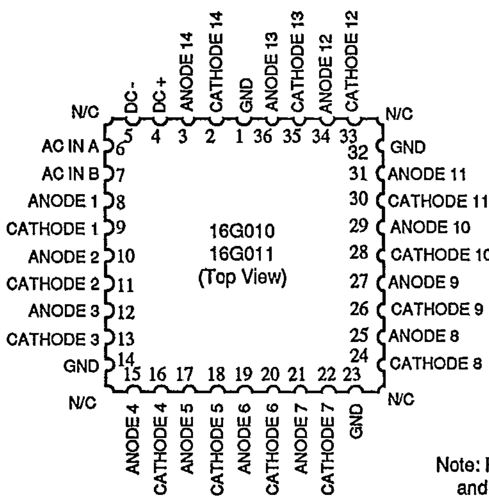
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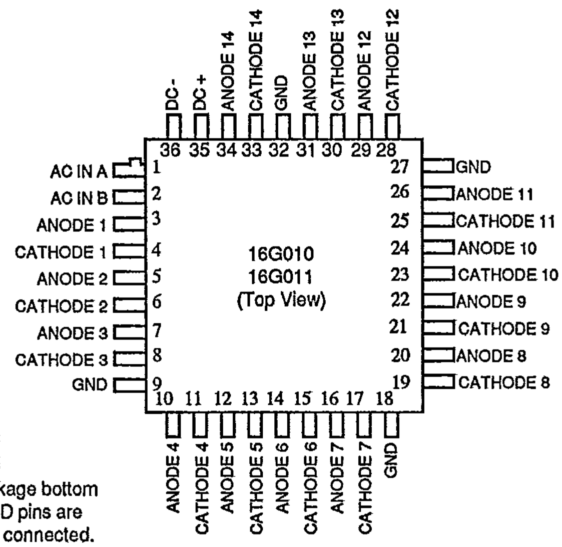
16G010
16G011

PIN FUNCTION DRAWINGS

36 I/O LEADLESS CHIP CARRIER
16G010-L36 and 16G011-L36



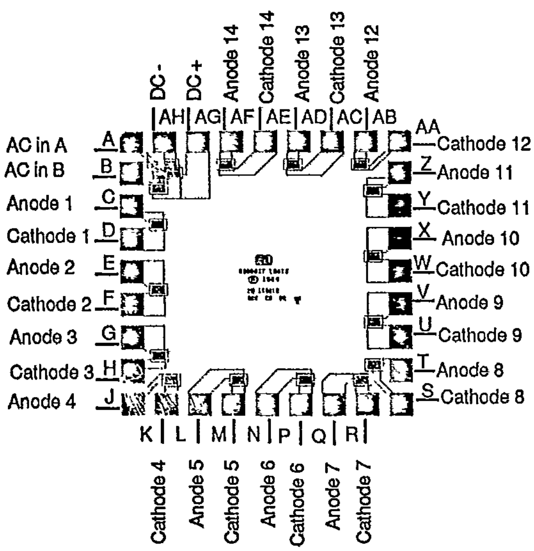
36 LEAD FLATPACK PACKAGE
16G010-F and 16G011-F



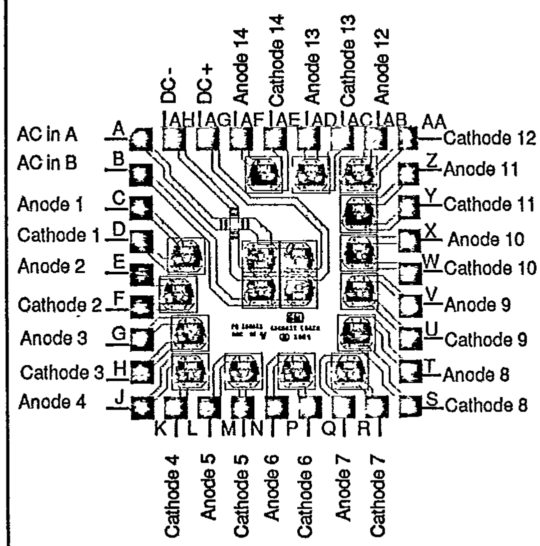
Note: Package bottom and GND pins are internally connected.

METALLIZATION AND PAD LAYOUT

16G010-X Die Size: 1.26 mm x 1.26 mm



16G011-X Die Size: 1.26 mm x 1.285 mm

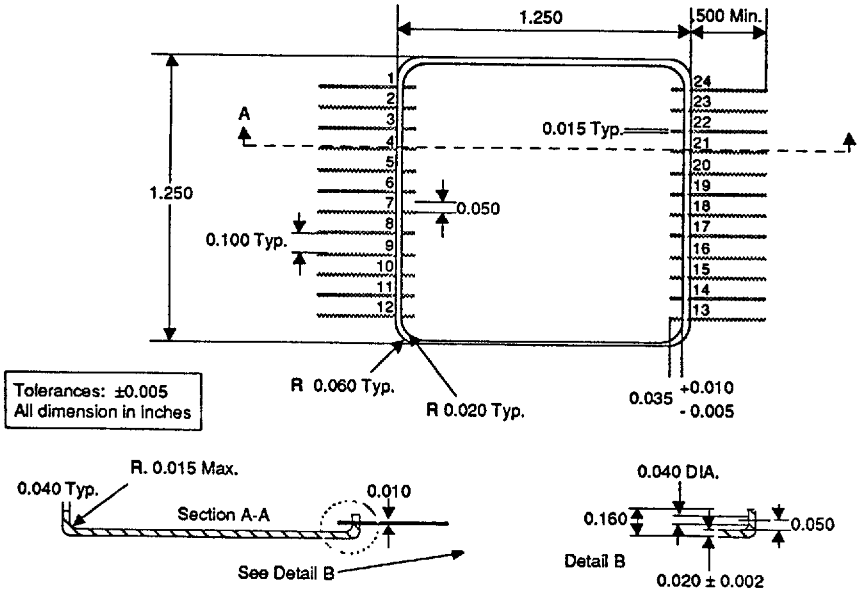


T-90-20

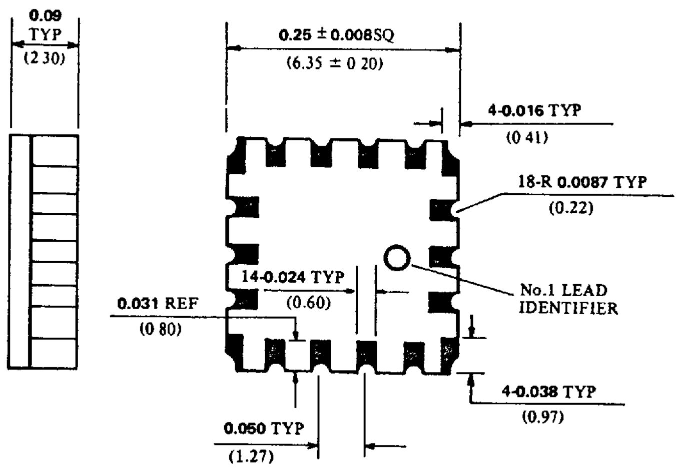
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24 PIN METAL FLATPACK 18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



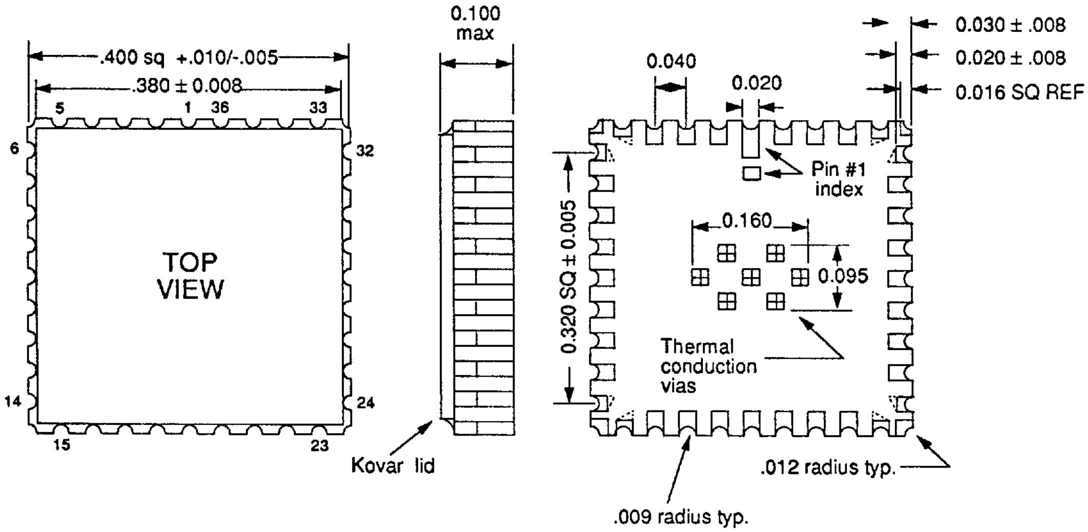
All dimensions shown in inches and (millimeters)

T-90-20

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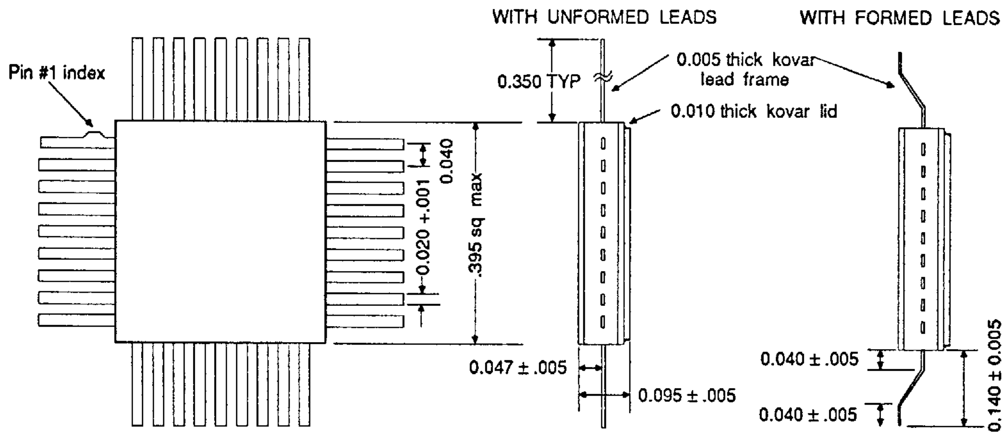
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F

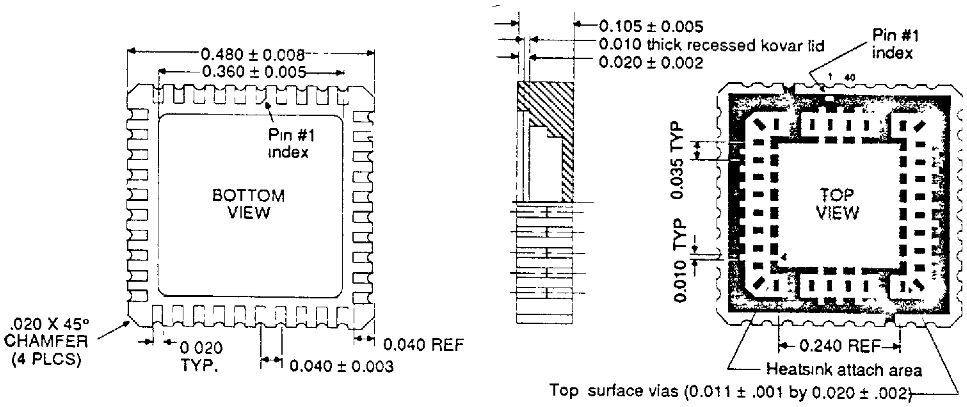


T-90-20

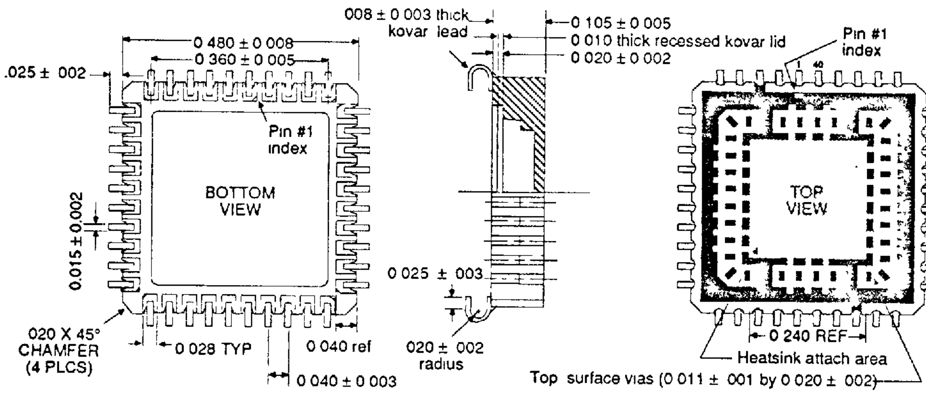
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40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

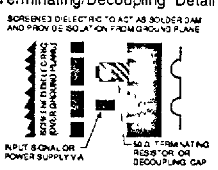


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip resistors are 0 040 long by 0 020 wide by 0 010 thick typ 100 mw min nominal power rating (Mini-Systems MSR 21 or equivalent)
(5) Recommended top surface chip capacitors are 0 040 long by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks are GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width

TOP SURFACE LEGEND	
Metalized Ceramic	■
Screened Dielectric	□
Bare Ceramic.	□

Top Surface Terminating/Decoupling Detail



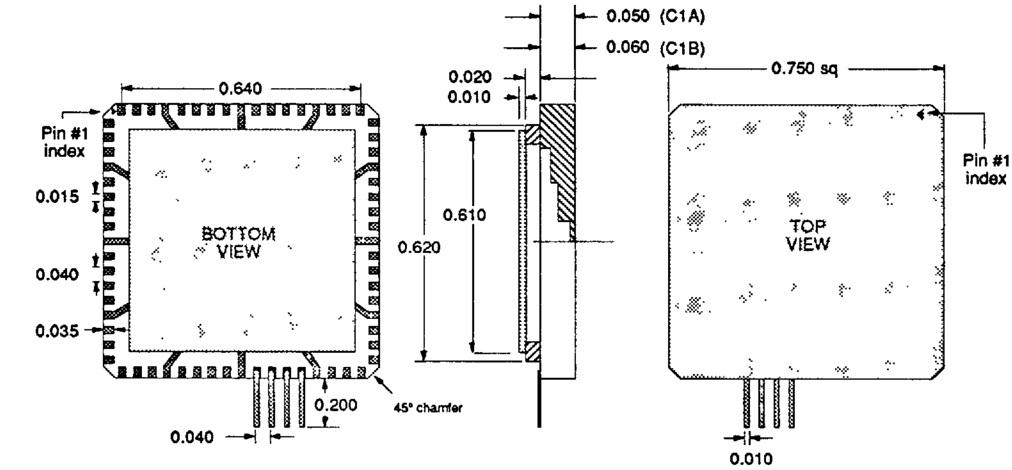
II

T-90-20

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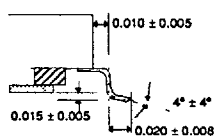
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3

